Advanced Passive Devices For Enhanced Integrated RF Circuit Performance

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Abstract **State of the art passive devices have been developed for optimum RF circuit performance. These devices include a hyperabrupt junction varactor with tunability (Cmax/Cmin) of 3.3, an accumulation mode MOS varactor, high capacitance nitride metal-insulator-metal capacitors, a BEOL TaN resistor and very high Q inductors with a peak Q of 28 at 3.5 Ghz. VCO simulations using several of these elements show a significant reduction in VCO gain variation, phase noise, and power consumption.**

I. Introduction

A suite of high quality passive elements built in SiGe BiCMOS technologies have been optimized to enhance the performance of monolithic wireless integrated circuits. These technical innovations improve circuit designs by reducing chip size and increase integration by incorporating passive elements that are traditionally off chip. The device design and fabrication strategy will be discussed for the following passive elements: a highly tunable hyperabrupt junction varactor, a MOS accumulation varactor, high capacitance nitride metal-insulator-metal (MIM) capacitors, a low tolerance metal resistor and parallel inductors with a very high quality factor. The impact of these elements on the circuit performance and area will be illustrated with a voltage controlled oscillator (VCO).

II. Passive Elements

Two varactors have been developed to augment the standard collector/base (CB) diode: a "hyperabrupt" enhancement of the CB diode and a MOS accumulation mode capacitor. The hyperabrupt (HA) varactor utilizes a retrograde implant to modify the CB junction. The resulting doping profile greatly enhances tunability and linearity, while retaining a high quality-factor Q. The tunability (Cmax/Cmin at 0 and 3V) of this device is excellent at 3.3 and is comparable to that of the MOS accumulation varactor as can be seen in Fig. 1. Moreover, Fig. 1 indicates that the HA varactor does not sacrifice linearity to achieve this tuning range.

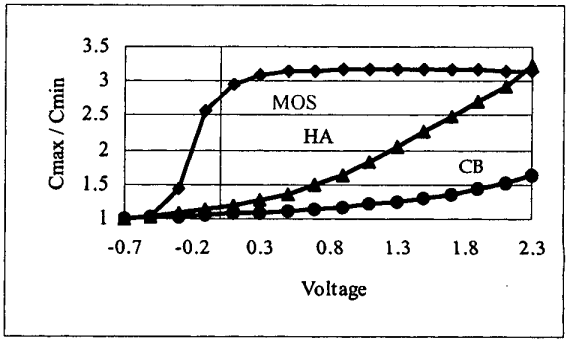

Fig. 1. CV curves for MOS accumulation varactor, HA junction varactor and standard collector base junction varactor.

Fig. 2, a plot of Q versus frequency for the HA varactor, demonstrates that the device has a quality factor in excess of 200 at 2 GHz. The MOS

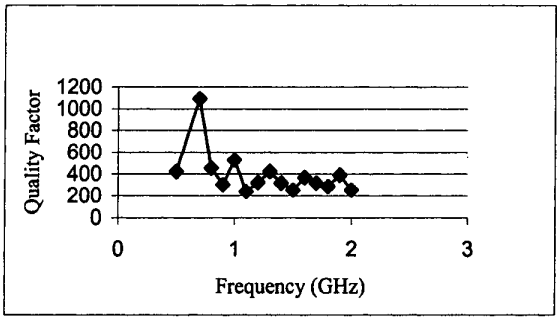

Fig. 2. Q vs Frequency for HA varactor.

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accumulation varactor is an n-channel MOSFET built in an N-well. Its capacitance is high in accumulation and decreases sharply in depletion.

Highly reliable aluminum MIM capacitors have been developed using PECVD nitride films. A novel integration scheme is used for parallel capacitors with capacitance densities as high as 2.7 fF/mm^2. The parametrics of a single capacitor with capacitance density of 1.35 fF/um^2 are shown in Table 1. The device has a Q of 150 at 2 Ghz, a very low TCR at 14.5 ppm/C, and is highly linear (voltage coefficient of 4 ppm/V). The single device has been qualified at 5.0 V for 100K power on hours use with up to 2 million um^2 per chip. The failure rate at 85 C is less than 10 ppm under these conditions.

TABLE 1
SUMMARY OF MIM PARAMETERS

Parameter	Value
Capacitance fF/um^2	1.35
Q at 2 GHz (100x100um Device)	150
TCR – ppm/C	14.5
Vcc – ppm/V	4

Precision TaN thin film resistors have been added to the existing suite of diffusion and polysilicon resistors used in our present SiGe BiCMOS technologies . The TaN film is deposited from a reactively sputtered Ta in N_2 ambient. The device can be produced in a copper or aluminum back end. The resistor has a sheet resistance of 140 ohms/sq and a tolerance of ±10% as shown in Table 2. The temperature coefficient of this device is -762 ppm/degree C. The parasitic capacitance of a TaN resistor produced in the BEOL is significantly reduced relative to a polysilicon resistor.

TABLE 2
SUMMARY OF TaN RESISTOR PARAMETRICS

Parameter	Value
TaN Rs – Ohms/Sq	140
Tolerance	10%
TCR – ppm/C	-762
Current Limit – mA/um	0.5
Area Cap. at Metal Level M1 – fF/um^2	0.025
Area Cap. – Polysilicon Resistor – fF/um^2	0.112

The performance of spiral inductors has been improved by thickening the spiral metal level and substituting Cu for Al to reduce series resistance. Fig. 3 shows Q curves for thick plated copper spirals from 4 to 33 um thick over an 8 um oxide dielectric. In each case, a 4 um underpass is used. The figure indicates that thickening the spiral metal continues to yield Q gains in spite of skin effect concerns. Thick spirals up to 33 um yield a quality facor in excess of 35 with no groundplane.

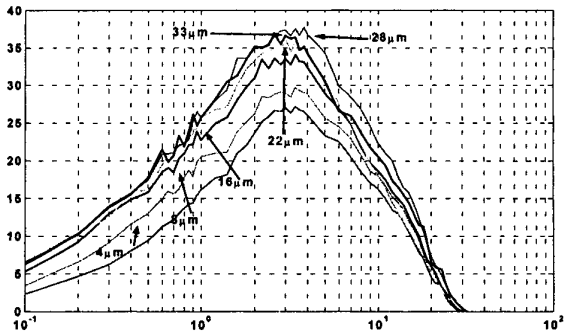

Fig. 3. Q vs Frequency for thick copper metal inductors.

The latest SiGe BiCMOS technology includes a two layer, low Rs metal stack (dual metal inductor) above the standard wire levels. The uppermost level is thick aluminum compatible with wire bonding or C4 attach, and the second level composed of thick copper. Each of these levels has an additional thick ILD layer below it (see Fig. 4).

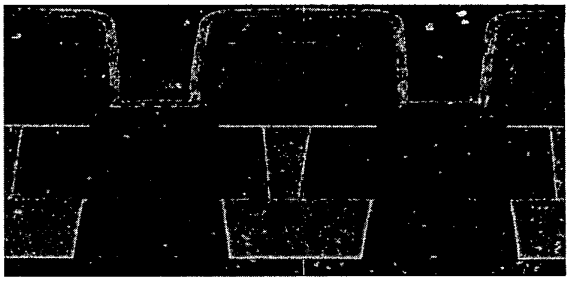

Fig. 4. Thick top aluminum layer and base copper layer used for dual metal inductors.

This configuration allows for very high Q inductors when wired in parallel. A peak Q of 28 is realized for a 1.1 nH inductor at 3.5 Ghz (see Fig. 5). Fig. 6 shows a comparison between the single level, parallel stacked,

and series stacked spiral inductance and Q results. This data indicates that a series inductor has an inductance density of roughly 3.6 X that of a single or parallel stacked inductor. This configuration allows for efficient inductor layouts and is a significant cost savings for inductor intense circuits. Efficient coupled structures such as transformers and baluns are also possible.

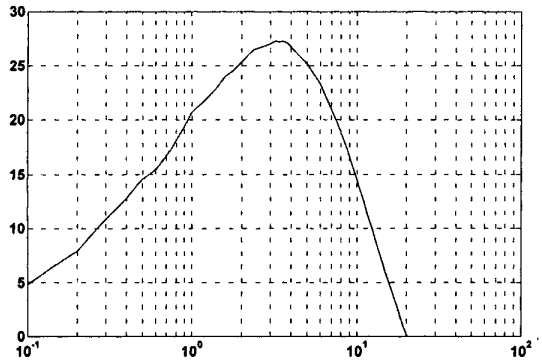

Fig. 5. Q (y axis) vs Frequency (x axis) for 1.1 nH dual metal inductor wired in parallel.

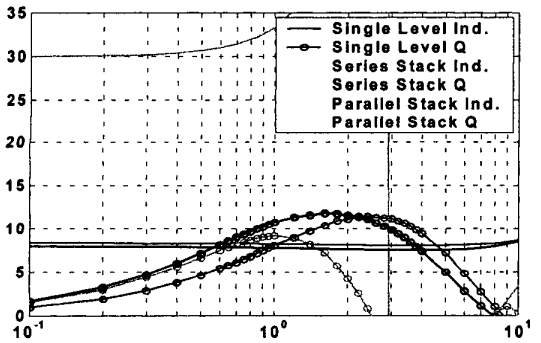

Fig. 6. Q and L (y-axis) for single level (red), series stacked (green) and parallel stack (blue) inductors as a function of frequency (x-axis).

III. VCO Circuit Simulations

Fully integrated Voltage Controlled Oscillators (VCOs) are a major bottleneck for system-on-chip (SOC) realization of wireless transceivers. High quality passive devices are required for the design of high performance VCOs. VCO parameters requiring high performance passive elements are phase noise, frequency tuning and VCO gain variation.

LC-tank voltage VCOs are a better choice than relaxation oscillators or ring oscillators to fulfill the required high frequency and phase noise specifications. The stringent phase noise of the VCO thus requires the integration of a high Q tank in an inherently high loss silicon substrate. For tank circuits, the inductor quality factor is usually much lower than that of the capacitor component (including varactors and other fixed capacitances), and therefore needs to be maximized. Both resistive loss of the metal and substrate loss contribute to the Q of inductors. While substrate loss can be minimized (or reduced) by using a differential inductor structure and using substrate shielding techniques in the circuit design, the metal loss is determined solely by the sheet resistance of the inductor. VCO circuits designed using parallel inductors in Fig. 4 have resulted in a 40% Q improvement versus a single low resistance aluminum inductor.

The frequency tunability of a VCO is decided by the capacitance tunability of the varactor. A tri-band GSM direct conversion system requires the VCO bandwidth to be about 10.5%. To cover this 10.5% frequency range over process and temperature variation, more than 20% of the frequency tuning range needs to be designed in the VCO. The standard base-collector junction varactor offered in our SiGe 5HP technology has a capacitance ratio of Cmax/Cmin=1.45 for a tuning voltage of 0.4V to 2.4V. With fixed capacitances from other active and passive devices unavoidable in the VCO circuit, this 20% frequency tuning range is very difficult to be achieved by the varactor, which is one of the major reasons that multiple band topology is utilized. The hyperabrupt junction varactor (HA) has a much larger capacitance tuning ratio: Cmax/Cmin=2.0 for the same 0.4V to 2.4V tuning voltage range. Using this HA varactor, a large bandwidth VCO is easily designed. VCO gain variation has great influence on the phase locked loop (PLL) performance. In a PLL frequency synthesizer, the VCO gain variation needs to be minimized. By doing so, the PLL loop bandwidth can be maintained relatively constant which will benefit the consistency of the PLL locking time and the phase noise of the PLL. The VCO gain is directly determined by the C-V performance of the varactor. Compared with the base collector junction varactor, the HA varactor provides significantly improved linear frequency tunability i.e., the VCO gain variation is reduced using the HA varactor as the frequency tuning device.

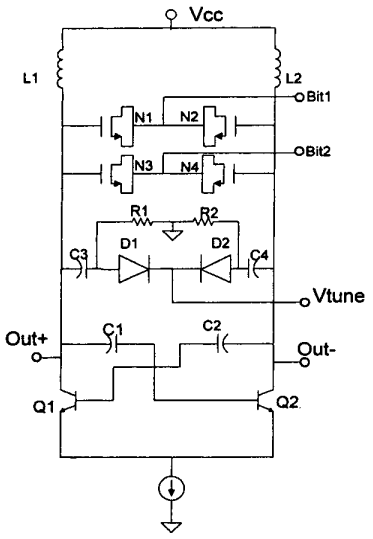

Fig. 7. Schematic of integrated VCO circuit.

In order to benchmark the advantage of these new passive devices in VCO design, the integrated VCO in Fig. 7 [1] has been redesigned using the dual metal inductors and HA varactor without any topology change. The original device was designed using a single thick Al layer for inductors and the standard CB junction varactor. Simulation results based upon hardware models are outstanding. The phase noise is improved by more than 2 dB with a 10% saving on power consumption. The VCO frequency tuning range is expanded to 24% from 21% and the VCO gain variation is reduced by 35% over the overall frequency tuning range.

IV. Conclusion

State of the art passive devices have been developed for optimum RF circuit performance. VCO simulations using these improved devices demonstrate significant performance improvements. Key figures of merit have been shown to demonstrate how these devices can be used to simultaneously improve RF circuit performance and reduce chip area.

References

[1] Xudong Wang, Dawn Wang, Kurt Schelkle, and Peter Bacon, " Fully Integrated Low Phase Noise VCO Design in SiGe BiCMOS Technology," Proceeding of the 2001 IEEE Radio and Wireless Conference, pp109-112, Boston, Aug. 2001.